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OFGS File No. : P/1909-130
Inventor : Yoshihiro KOTA
Title : MEMORY ADDRESS SPACE EXTENSION DEVICE AND STORAGE MEDIUM STORING THEREIN PROGRAM THEREOF
Assignee : NEC Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

95 Pages of Specification including Abstract and Claims
293 Numbered Claims Calculated as 293 Claims for Fee Purposes
8 Sheets of Drawing Containing Figures 1 to 11.
X Declaration and Power of Attorney
X Priority is Claimed under 35 U.S.C. §119:
Convention Date April 20, 1999 for Japan appln. S.N. 11-112368
Convention Date January 19, 2000 for Japan appln. S.N. 2000-014102
X Two Certified Priority Applications
Verified Statement Claiming Small Entity Status under 37 C.F.R. §1.27.
X Assignment
X Return-Addressed Post Card

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MEMORY ADDRESS SPACE EXTENSION DEVICE AND STORAGE MEDIUM STORING THEREIN PROGRAM THEREOF

BACKGROUND OF THE INVENTION

The present invention relates to a memory address space extension device and a storage medium storing therein a program thereof in which the memory address space extension device converts a CPU (central processing unit) address into an extended address and the program executes processing memory address space extension.

Description of the Prior Art

A conventional memory address extension device includes a register bank in every task. The register bank consists of a plurality of page registers which are combined therewith. The page register stores therein CPU (central processing unit) address and upward address of extended address which is broader than the CPU address. When task switch occurs, the memory address extension device extends memory address space in such a way of causing the register bank to be switched.

However, in the conventional technique described above, on the supposition that there exists a data to which only certain task accesses. However, another task capable of accessing such the data to which only determined certain task should access. Therefore, there is the problem that the data which should only be accessed by the determined certain task is capable of being rewritten wrongly by the another task.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present invention, in order to overcome the above mentioned problem, to provide a memory address space extension device and a storage medium storing therein a program thereof which enable rewrite data wrongly according to task to be prevented in order to protect the data.

It is another object of the present invention, to provide a memory address space extension device and a storage medium storing therein a program thereof enable the data to which only certain task should access to be prevented from accessing wrongly by interruption processing to such the data in order to protect it.

According to a first aspect of the present invention, in order to achieve the above mentioned object, there is provided a memory address space extension device which comprises a definition table for defining an access right of a task ID (identification) with respect to a data area, a task ID register for storing therein the task ID of a task during execution, an extraction means for extracting a data area ID from a CPU (central processing unit) address inputted previously, a judgement means for judging as to whether or not it is capable of being permitted that the task during execution indicated by the task ID accesses the data area indicated by the data area ID while referring to the definition table from both of data area ID extracted previously and the task ID stored in the task ID register.

According to a second aspect of the present invention, in the first aspect, there is provided a memory address space extension device, wherein there are provided an address operational means for converting the CPU address into an extended address, and a memory having the extended address converted previously, when the judgement means judges that judgement result according to the judgement means is a result that the task during execution accesses the data area, the address operational means executes the conversion processing.

According to a third aspect of the present invention, in the first aspect, there is provided a memory address space extension device, wherein, as to the definition table, it causes combination that access is permissible or in-permissible with respect to read and / or write to the data area respectively to be defined.

According to a fourth aspect of the present invention, in the first aspect, there is provided a memory address space extension device, wherein there is provided a forming means for forming said definition table.

According to a fifth aspect of the present invention, there is provided a storage medium for storing therein a program in order to execute the processing of a storing processing for storing a task ID of a task during execution, an extraction processing for extracting a data area ID from a CPU address inputted previously, and a processing for judging as to whether or not it is capable of being permitted that the task during execution indicated by the task ID accesses the data area indicated by the data area ID while referring to the definition table from both of data area ID extracted previously and the task ID stored in the task ID register.

According to a sixth aspect of the present invention, in the fifth aspect, there is provided a storage medium for storing therein a program, wherein the program executes the processing of an address operational processing for converting the CPU address into an extended address when judgement result according to the judgement processing is that the task is permitted that the task during execution accesses the data area.

According to a seventh aspect of the present invention, in the sixth aspect, there is provided a memory address space extension device which comprises a definition table for defining an access right of a task with respect to a data area, and an access right judgement means for judging whether or not it causes the access right to the data area which the task requests to be given with respect to the task according to the definition table.

According to an eighth aspect of the present invention, in the seventh aspect, there is provided a memory address space extension device, wherein the definition table defines as to whether or not the task possesses an access right for accessing prescribed data area in every task

ID given to the task.

According to a ninth aspect of the present invention, in the seventh aspect, there is provided a memory address space extension device, wherein the definition table defines as to whether or not said task possesses an access right for accessing prescribed data area in every task ID given to the task and / or in every interruption number given to interruption processing.

According to a tenth aspect of the present invention, in the seventh or eighth aspect, there is provided a memory address space extension device, wherein the access right judgement means judges whether it causes the access right to the data area requested by the task to be given according to the task ID, and the data area ID indicating the data area requested by the task.

According to an eleventh aspect of the present invention, in the seventh or ninth aspect, there is provided a memory address space extension device, wherein the access right judgement means judges whether it causes the access right to the data area requested by the task to be given according to any one of the task ID and the interruption processing number, and according to the data area ID indicating the data area requested by the task.

According to a twelfth aspect of the present invention, in any one of the seventh to the eleventh aspects, there is provided a memory address space extension device, wherein the definition table defines whether or not it causes access to be permitted with respect to the prescribed data area in every the task.

According to a thirteenth aspect of the present invention, in any one of the seventh to the eleventh aspects, there is provided a memory address space extension device, wherein the definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to the prescribed data area in every said task.

According to a fourteenth aspect of the present invention, in any one of the ninth, the eleventh, the twelfth, and the thirteenth aspects, there is provided a memory address space extension device, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

According to a fifteenth aspect of the invention, in any one of the ninth, the eleventh, the twelfth, the thirteenth, and the fourteenth aspects, there is provided a memory address space extension device, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to the interruption instruction according to software.

According to a sixteenth aspect of the present invention, in any one of the seventh to the fifteenth aspects, there is provided a memory address space extension device, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein the address operational means causes the CPU address to be converted into the extended address when the task is permitted to access to the data area according to the access right judgement means.

According to a seventeenth aspect of the present invention, in any one of the seventh to the sixteenth aspects, there is provided a memory address space extension device wherein there is further provided a

definition table forming means for forming the definition table.

According to an eighteenth aspect of the present invention, there is provided a storage medium storing therein a program in order to execute the processing of a definition table preparation processing for preparing a definition table, a reference processing for the sake of the definition table which defines an access right of a task with respect to data area, and an access right judgement processing for judging whether or not it causes the access right for the data area requested by a task to be given to the task according to the definition table.

According to a nineteenth aspect of the present invention, in the eighteenth aspect, there is provided a storage medium storing therein a program, wherein the reference processing for definition table is the reference processing that it causes the definition table defining whether or not the task possesses the access right for accessing prescribed data area to be seen in every task ID given to the task.

According to a twentieth aspect of the present invention, in the eighteenth aspect, there is provided a storage medium storing therein a program, wherein the reference processing for definition table is the reference processing that it causes the definition table defining whether or not the task possesses the access right for accessing prescribed data area to be seen in every task ID given to the task and / or in every interruption number given to the interruption processing.

According to a twenty-first aspect of the present invention, in the eighteenth or nineteenth aspects, there is provided a storage medium storing therein a program, wherein the access right judgement processing judges whether or not the task possesses the access right for accessing prescribed data area according to the task ID and / or the data area ID indicating the data area requested by the task.

According to a twenty-second aspect of the present invention, in the eighteenth or the twentieth aspect, there is provided a storage

medium storing therein a program, wherein the access right judgement processing judges whether or not the task possesses the access right for accessing prescribed data area according to any one of the task ID and the interruption processing number and / or the data area ID indicating the data area requested by the task.

According to a twenty-third aspect of the present invention, in any one of the eighteenth to the twenty-second aspects, there is provided a storage medium storing therein a program, wherein the reference processing for definition table is the reference processing that it causes the definition table defining whether or not the task possesses the access right for accessing prescribed data area to be seen in every the task.

According to a twenty-fourth aspect of the present invention, in any one of the eighteenth to the twenty-second aspects, there is provided a storage medium storing therein a program, wherein the program executes the reference processing for definition table, which is the reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to the prescribed data area in every the task.

According to a twenty-fifth aspect of the present invention, in any one of the twentieth, the twenty-second, the twenty-third, and the twenty-fourth aspects, there is provided a storage medium storing therein a program, wherein the program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

According to a twenty-sixth aspect of the present invention, in any one of the twentieth, the twenty-second, the twenty-third, the twenty-

fourth, and twenty-fifth aspects, there is provided a storage medium storing therein a program, wherein the program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

According to a twenty-seventh aspect of the present invention, in any one of the eighteenth to the twenty-sixth aspects, there is provided a storage medium storing therein a program, wherein the program executes an address operational processing in order to convert a CPU address into an extended address in such a way that the address operational processing causes the CPU address to be converted into the extended address when the task is judged that the task is permitted to access to the data area according to the access right judgement processing, before executing storage processing of the converted address into a memory.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with the accompanying drawings. It should be expressly understood, however, that the drawings are for purpose of illustration only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a first block diagram showing a configuration of a memory address space extension device in an embodiment of the present invention;

Fig. 2 is a block diagram showing a configuration of an address operational unit in the embodiment of the present invention;

Fig. 3 is a constitution view showing register bank selection table in the embodiment of the present invention;

Fig. 4 is a first data area access right definition table in the

embodiment of the present invention;

Fig. 5 is a constitution view in the case of forming execution form file from data class definition file in the embodiment of the present invention;

Fig. 6 is a second data area access right definition table in the embodiment of the present invention;

Fig. 7 is a second block diagram showing a configuration of the memory address space extension device in the embodiment of the present invention;

Fig. 8 is a third data area access right definition table in the embodiment of the present invention;

Fig. 9 is a fourth data area access right definition table in the embodiment of the present invention;

Fig. 10 is a flowchart explaining a first operation of the memory address space extension device in the embodiment of the present invention; and

Fig. 11 is a flowchart explaining a second operation of the memory address space extension device in the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will be described in detail accompanying the drawings.

Fig. 1 is a block diagram showing a first embodiment of a memory address space extension device according to the present invention.

In Fig. 1, the memory address space extension device comprises a CPU1 having a certain address space, a memory 2 having extended address which is broader address space than that of the CPU1, and a memory management unit (hereinafter referred to as MMU) 3.

The MMU3 consists of a task ID register 4 storing therein the task

ID of a task with execution conditions, and an address operational unit 5 converting a CPU address into an extended address.

Fig. 2 is a constitution of the address operational unit 5 of Fig. 1.

In Fig. 2, the address operational unit 5 consists of a page register 7 for storing page register data necessary for calculating the extended address, a plurality of register banks 6 which are combined to be constituted by a plurality of the page registers 7, a register bank control unit 8 for obtaining register bank number from both of data area ID which is a part of the CPU address and task ID, and a cache 9.

The cache 9 accommodates both of a register bank selection table 10 as shown in Fig. 3 and a data area access right definition table 11 as shown in Fig. 4.

(FIRST OPERATION)

Next, there will be explained operation.

The address operational unit 5 inputs therein the CPU address from the CPU1. The CPU address consists of data area ID, register bank address, and offset address.

The address operational unit 5 decomposes the inputted CPU address into above data area ID, a register bank address, and an offset in order to extract thereof (STEP S102). Next, a register bank control unit 8 refers to the data area access right definition table 11 existing in the cache 9. The task ID is stored in the task ID register 4. It causes the access right for the data area to be requested to the task during execution from both of the task ID stored in the task ID register 4 and the data area ID which is extracted (STEP S103). When the access is not permitted (STEP S103/NO), the access is not executed to the data area, thus system error occurs (STEP S105).

When the access is permitted (STEP S103/YES), it causes the register bank number of the data area which is attempted to access to be obtained while referring to the register bank selection table 10 existing in

the cache 9 (STEP S104). The address operational unit 5 fetches a page register data stored in the page register while selecting the page register from the register bank address. The address operational unit 5 obtains an extended address from the register bank number obtained previously, the page register, and the offset address (STEP S106).

According to such procedure, it is capable of preventing data area from wrongly accessing by the task which is not permitted the access. Consequently, it is capable of protecting the data from accessing wrongly by the task which is not permitted accessing thereto.

Next, there will be described operation of the present embodiment while using concrete example.

As shown in Fig. 5, a linker / locator 12 forms an execution form file from among an object file, a data class causing a plurality of data to be gathered, and a data class definition file causing access right of such data class to be defined (STEP S100). On this occasion, the data class arranges the same data while putting them in order. Further, as shown in Fig. 4, on the supposition that the task ID includes the tasks 1, 2, 3, and 4, and the data areas A, B, and C exist. The access right of respective tasks for the respective data areas is shown in Fig. 4.

Firstly, on the occasion of the initialization, it causes both of a register bank selection table 10 and a data area access right definition table 11 to be formed in the cache 9 (STEP S101).

The CPU 1 executes data access instruction. On this occasion, the address operational unit 5 decomposes the CPU address into the data area ID, the register bank address, and the offset (STEP S102). Next, a register bank control unit 8 refers to the data area access right definition table 11 existing in the cache 9. The register bank control unit 8 requests the access right for the data area with respect to the task during execution from both of the task ID stored in the ID register 4 and the above described data area ID (STEP S103).

As shown in Fig. 4, when the task whose task ID is 1 (one) attempted to read the data existing in the data area B, since the access right is not permitted (STEP S103 / NO), the access to the data area B is not executed, thus the system error occurs (STEP S105). When the task whose task ID is 1 (one) attempted to rewrite the data existing in the data area A, since the access right is permitted (STEP S103 / YES), it causes the register bank number of the data area attempting to access to be obtained while referring to the register bank selection table 10 existing in the cache 9 (STEP S104).

The address operational unit 5 selects the page register from the register bank number obtained previously and the register bank address, thus obtaining the extended address from both of the page register data stored in the register bank address and the offset address (STEP S106).

(SECOND OPERATION)

Fig. 6 shows constitution of the data area access right definition table 11 according to the second embodiment of the present invention. Furthermore, the constitution of the memory address space extension device is the same as that of Fig. 1.

In the first embodiment, the access right of the data area access right definition table 11 of Fig. 4 is only "permissible" or "in-permissible". However, in the present embodiment, as shown in Fig.6, there are four kinds of the access right of the data area access right definition table 11. The four kinds of the access rights are "readable, in-writable", "in-readable, writable", "readable, writable", and "in-readable, in-writable". These points are different from the first embodiment.

Next, there will be explained operation of the present embodiment using concrete example.

When the task whose task ID is 1 (one) attempted to read the data existing in the data area B, since the access right of the data area access right definition table 11 of Fig. 6 is impermissible, it causes the access for

the data area B to be not implemented, thus the system error occurs. While when the task whose task ID is 1 (one) attempted to rewrite the data existing in the data area A, since the access right of the data area access right definition table 11 of Fig. 6 is permissible, it causes the register bank number to be obtained while referring to the register bank selection table 10 existing in the cache 9.

Further, a storage unit such as ROM (read only memory) and so forth storing therein a program in a computer system constitutes the memory address space extension device of Fig. 1. Thus the storage unit of the ROM and so forth constitutes a storage medium according to the present invention. The storage medium stores therein the program indicating processing in order to execute operation described in the above respective embodiment.

It is capable of being used an optical disk, a magneto-optical disk, a magnetic recording medium, a semiconductor memory, and so forth as the storage medium.

(THIRD OPERATION)

Fig. 7 is a second block diagram showing constitution of the memory address space extension device in the embodiment of the present invention. The memory address space extension device shown in Fig. 7 comprises a CPU 71, a memory 72, a memory management unit (MMU) 73, and an interruption control unit (ICU) 76.

The CPU 71 possesses prescribed address space. The memory 72 possesses an extended address which is address space broader than address space which the CPU 71 possesses.

Further, the memory management unit (MMU) 73 consists of a task ID register 74, an address operational unit 75, and a decoder 77.

The task ID register 74 accommodates task ID of a task which is effective condition. The task ID register 74 accommodates an interruption number of interruption processing during execution too.

The address operational unit 75 converts the CPU address into the extended address. The interruption control unit (ICU) 76 produces interruption according to hardware.

Fig. 7 shows the memory address space extension device. Operation in which it causes the extended address to be obtained will be explained in detail referring to Figs. 2, 3, 5, 7, and 11. The extended address is obtained with respect to the task that is under the condition that access in relation to a certain data area is not permitted. The extended address is also obtained with respect to the task which is under the condition that access is permitted, while preventing wrong access according to interruption processing.

As shown in Fig. 5, on the inside of the memory address space extension device, the linker / locator forms the execution form file from among the object file, the data class in which a plurality of data is gathered, the data class definition file which defines the access right of such the data class (STEP S110). On this occasion, the data whose data class is identical therewith is arranged while collecting.

Fig. 8 is a third data area access right definition table in the embodiment of the present invention. As shown in Fig. 8, with respect to the present embodiment, on the supposition that the task of "101", "102", "103", and "104" exists as the task ID, the interruption processing of "1", "2", and "3" exists as the interruption number. Further, on the supposition that there exists "area A", "area B", and "area C" as the data area.

The interruption processing of the interruption numbers "1" and "2" is taken to be the interruption processing according to software. The interruption processing of the interruption number "3" is taken to be the interruption processing according to hardware.

The memory address space extension device shown in Fig. 7 forms the register bank selection table shown in Fig. 3 to the cache 11 on the

occasion of initialization. The memory address space extension device also forms the data area access right definition table shown in Fig. 8 to the cache 11 on the occasion of initialization (STEP S111).

When the system operates, OS (Operating System) accommodates the task ID of the task which is under effective condition into the task ID register 74. When the task switch occurs, the OS accommodates the task ID which becomes effective condition according to the task switch into the task ID register 74.

The interruption according to hardware occurs during system operation. On this occasion, the interruption control unit (ICU) 76 produces interruption number. The produced interruption number is accommodated in the task ID register.

The CPU 71 causes the interruption instruction according to the software to be executed. On this occasion. the interruption number which is decoded by the decoder 77 is accommodated in the task ID register 74.

Furthermore, when the instruction for returning from the interruption processing is executed, the CPU 71 accommodates the task ID of the task which is in the effective condition immediately before execution of the interruption processing into the task ID register 74.

The address operational unit 75 decomposes the CPU address inputted from the CPU 71 into the data area ID, the register bank address, and the offset (STEP S112).

The register bank control unit 8 in the address operational unit 75 refers to a data area access right definition table 81 shown in Fig. 8 accommodated the cache 11 according to the task ID stored in the task ID register, or the interruption number and the above described data area ID, thus the register bank control unit 8 requests the access right for the data area with respect to the task during execution (STEP S113).

When the interruption processing of the interruption number "1"

is attempted to read the data existing in the area "B", the interruption processing of the interruption number "1" does not possess such the access right according to the data area access right definition table shown in Fig. 8 (STEP S 113 / NO).

Consequently, the memory address space extension device shown in Fig. 7 does not execute the access to the data area "B". Namely, the interruption processing of the interruption number "1" described above becomes the system error (STEP S115).

When the interruption processing of the interruption number "1" is attempted to rewrite the data existing in the area "A", the interruption processing of the interruption number "1" is permitted about the access to the data area "A" according to the data area access right definition table 81 shown in Fig. 8 (STEP S113 / YES). Consequently, the register bank control unit 8 refers to the register bank selection table 12 within the cache 11 shown in Fig. 3. The register bank control unit 8 requests the register bank number of the data area [area "A"] which is attempted to access by the above interruption processing (the interruption processing of the interruption number "1") (STEP S114).

The address operational unit 75 selects a page register 7 from among the above register bank number, and the above register bank address. The address operational unit 75 obtains the extended address from among the page register data stored in the page register 7, and the above described offset address (STEP S116).

Furthermore, a storage unit such as ROM (read only memory) and so forth storing therein a program in a computer system constitutes the memory address space extension device of Fig. 7. Thus the storage unit of the ROM and so forth constitutes a storage medium according to the present invention. The storage medium stores therein the program indicating processing in order to execute operation described in the above respective embodiment.

It is capable of being used an optical disk, a magneto-optical disk, a magnetic recording medium, a semiconductor memory, and so forth as the storage medium.

According to the first operational example described above, the task ID register stores therein the task ID of the task during execution. Consequently, in the case of the interruption processing, value of the task ID register is not changed. For that reason, the interruption processing becomes capable of accessing to the data to which only predetermined certain task accesses.

Namely, according to the above described first operational example, there exits a data to which only prescribed task is permitted to access. It is incapable of preventing that the wrong interruption processing accesses to such the data.

However, according to the above described third operational example, it causes wrong access to be prevented from the task that the access is not permitted with respect to certain data area. Further, it becomes possible to prevent wrong access according to the interruption processing with respect to certain data area. As a result thereof, reliability of the data is improved in the above data area.

(FOURTH OPERATION)

Fig. 8 is view showing the fourth data area access right definition table in the embodiment of the present invention. Hereinafter, there will be described operation of preventing wrong access referring to Figs. 2, 7, and 9. The memory address space extension device shown in Fig. 7 enable the wrong access to be prevented from the task which is not permitted access with respect to certain data area. Also, the memory address space extension device enable wrong access according to the interruption processing to be prevented.

Furthermore, the fourth operational example differs from the third operational example described above. The different point is

processing concerning the access right judgement of either the task during execution or the interruption processing (processing of STEP S113 shown in Fig. 11). Thus, there will be described with respect to this processing.

The fourth operational example differs from the third operational example in the data area access right definition table. The data area access right definition table 81 shown in Fig. 8 indicates area to which the access right is permitted in every task ID, or in every interruption number.

By contrast, the data area access right definition table 91 shown in Fig. 9 defines the access right with respect to the area that it is capable of executing only write of the data in every task ID, or in every interruption number (In Fig. 9, referred to as "W"). The data area access right definition table defines the access right with respect to the area that it is capable of executing only read of the data (In Fig. 9, referred to as "R"). The data area access right definition table defines the access right with respect to the area that it is capable of executing both of read of the data, and write of the data (In Fig. 9, referred to as "RW").

According to Fig. 9, the interruption processing of the interruption number "1" (one), in the case of attempting to read the data existing in the data area "B", the access right is not recognized (according to Fig. 9, defined as "×"). Consequently, the memory address extension device shown in Fig. 7, does not execute access with respect to the data area "B", but it causes the operation to be terminated as the system error.

According to Fig. 9, the interruption processing of the interruption number "1" (one), in the case of attempting to read the data existing in the data area "A", the access right is recognized (according to Fig. 9, defined as "R"). Consequently, the memory address space extension device shown in Fig. 7 refers to the register bank selection table 12 existing in the cache 11 shown in Fig. 3, before requesting the register bank number

of the data area "A" to which the interruption processing of the above interruption number "1" attempts to access.

Furthermore, the storage unit such as ROM (read only memory) and so forth storing therein the program in the computer system constituting the memory address space extension device of Fig. 7 constitutes the storage medium according to the present invention. The storage medium stores therein the program indicating processing in order to execute operation explained on the respective embodiments described-above.

It is capable of being used an optical disk, a magneto-optical disk, a magnetic recording medium, a semiconductor memory, and so forth as the storage medium.

The fourth operational example is compared with the above third operational example. According to the fourth operational example, it becomes possible to implement more detailed access restriction in every task, or in every interruption processing. As a result thereof, reliability of the data is further improved.

As described above according to the present invention, there is provided the table of defining that the access right is permissible or the access right is in-permissible by the task with respect to certain data area. Thus, it is capable of preventing wrong access from the task with respect to a certain data area. For that reason, it is capable of protecting the data of the area, thus, it is capable of improving the reliability of the data.

Further, according to the present invention, there is provided the table of defining that the access right is permissible or the access right is in-permissible by the task with respect to certain data area or the interruption processing. Thus, it is capable of preventing wrong access from the task with respect to a certain data area and / or the interruption processing. For that reason, it is capable of protecting the data of the area, thus, it is capable of improving the reliability of the data.

Furthermore, in the above described definition table, it causes combination that the read, and the write with respect to the data area are permissible or in-permissible respectively to be defined, thus it is capable of executing fine-grained control in answer to the inputted CPU data.

While preferred embodiments of the invention have been described using specific terms, the description has been for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of following claims.

WHAT IS CLAIMED IS:

1. A memory address space extension device comprising:

a definition table defining an access right of a task ID (identification) with respect to data area;

a task ID register for storing therein the task ID of a task during execution;

an extraction means for extracting a data area ID from a CPU (central processing unit) address inputted previously;

a judgement means for judging as to whether or not it is capable of being permitted that the task during execution indicated by the task ID accesses the data area indicated by the data area ID while referring to said definition table from both of data area ID extracted previously and the task ID stored in said task ID register.

2. A memory address space extension device as claimed in claim 1, wherein there are provided an address operational means for converting said CPU address into an extended address, and a memory having the extended address converted previously, when said judgement means judges that judgement result according to said judgement means is a result that the task during execution accesses the data area, said address operational means executes said conversion processing while causing said memory with extended address to support.

3. A memory address space extension device as claimed in claim 1, wherein, as to said definition table, it causes combination that access is permissible or in-permissible with respect to read and / or write to said data area respectively to be defined.

4. A memory address space extension device as claimed in claim 1, wherein there is provided a preparation means for preparing said

definition table.

5. A storage medium for storing therein a program in order to execute the processing of:

a storing processing for storing a task ID of a task during execution;

an extraction processing for extracting a data area ID from a CPU address inputted previously; and

a processing for judging as to whether or not it is capable of being permitted that the task during execution indicated by the task ID accesses the data area indicated by the data area ID while referring to said definition table from both of data area ID extracted previously and the task ID stored in said task ID register.

6. A storage medium for storing therein a program as claimed in claim 5, wherein said program executes the processing of an address operational processing for converting said CPU address into an extended address when judgement result according to said judgement processing is that the task is permitted that the task during execution accesses the data area.

7. A memory address space extension device comprising:

a definition table forming means for forming said definition table;

a definition table for defining an access right of a task with respect to a data area; and

an access right judgement means for judging whether or not it causes the access right to the data area requested by the task to be given with respect to the task according to said definition table.

8. A memory address space extension device as claimed in claim

7, wherein said definition table defines as to whether or not said task possesses an access right for accessing prescribed data area in every task ID given to the task.

9. A memory address space extension device as claimed in claim 7, wherein said definition table defines as to whether or not said task possesses an access right for accessing prescribed data area in every task ID given to the task and / or in every interruption number given to interruption processing.

10. A memory address space extension device as claimed in claim 7, wherein said access right judgement means judges whether it causes the access right to the data area requested by said task to be given according to said task ID, and the data area ID indicating the data area requested by said task.

11. A memory address space extension device as claimed in claim 8, wherein said access right judgement means judges whether it causes the access right to the data area requested by said task to be given according to said task ID, and the data area ID indicating the data area requested by said task.

12. A memory address space extension device as claimed in claim 7, wherein said access right judgement means judges whether it causes the access right to the data area requested by said task to be given according to any one of said task ID and said interruption processing number, and according to the data area ID indicating the data area requested by said task.

13. A memory address space extension device as claimed in claim

9, wherein said access right judgement means judges whether it causes the access right to the data area requested by said task to be given according to any one of said task ID and said interruption processing number, and according to the data area ID indicating the data area requested by said task.

14. A memory address space extension device as claimed in claim 7, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

15. A memory address space extension device as claimed in claim 8, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

16. A memory address space extension device as claimed in claim 9, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

17. A memory address space extension device as claimed in claim 10, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

18. A memory address space extension device as claimed in claim 11, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

19. A memory address space extension device as claimed in claim 12, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

20. A memory address space extension device as claimed in claim 13, wherein said definition table defines whether or not it causes access to be permitted with respect to said prescribed data area in every said task.

21. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

22. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

23. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

24. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

25. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

26. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

27. A memory address space extension device as claimed in claim 7, wherein said definition table defines any one of:

(1) causing only write of the data to be permitted;

(2) causing read of the data to be permitted;

(3) causing write of the data and read of the data to be permitted; and

(4) causing no-access to be permitted,

with respect to said prescribed data area in every said task.

28. A memory address space extension device as claimed in claim 9, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

29. A memory address space extension device as claimed in claim 12, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

30. A memory address space extension device as claimed in claim 13, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

31. A memory address space extension device as claimed in claim 14, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

32. A memory address space extension device as claimed in claim 15, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

33. A memory address space extension device as claimed in claim 16, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

34. A memory address space extension device as claimed in claim 17, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

35. A memory address space extension device as claimed in claim 18, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

36. A memory address space extension device as claimed in claim 19, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

37. A memory address space extension device as claimed in claim 20, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

38. A memory address space extension device as claimed in claim 21, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

39. A memory address space extension device as claimed in claim 22, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

40. A memory address space extension device as claimed in claim 23, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

41. A memory address space extension device as claimed in claim 24, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

42. A memory address space extension device as claimed in claim 25, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

43. A memory address space extension device as claimed in claim 26, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

44. A memory address space extension device as claimed in claim 27, wherein there is further provided an interruption number generation means for generating interruption number with respect to interruption processing according to hardware.

45. A memory address space extension device as claimed in claim 9, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

46. A memory address space extension device as claimed in claim 12, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

47. A memory address space extension device as claimed in claim 13, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

48. A memory address space extension device as claimed in claim 14, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

49. A memory address space extension device as claimed in claim 15, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

50. A memory address space extension device as claimed in claim 16, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

51. A memory address space extension device as claimed in claim 17, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

52. A memory address space extension device as claimed in claim 18, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

53. A memory address space extension device as claimed in claim 19, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

54. A memory address space extension device as claimed in claim 20, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

55. A memory address space extension device as claimed in claim 21, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

56. A memory address space extension device as claimed in claim 22, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

57. A memory address space extension device as claimed in claim 23, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

58. A memory address space extension device as claimed in claim 24, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

59. A memory address space extension device as claimed in claim 25, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

60. A memory address space extension device as claimed in claim 26, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

61. A memory address space extension device as claimed in claim 27, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

62. A memory address space extension device as claimed in claim 28, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

63. A memory address space extension device as claimed in claim 29, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

64. A memory address space extension device as claimed in claim 30, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

65. A memory address space extension device as claimed in claim 31, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

66. A memory address space extension device as claimed in claim 32, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

67. A memory address space extension device as claimed in claim 33, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

68. A memory address space extension device as claimed in claim 34, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

69. A memory address space extension device as claimed in claim 35, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

70. A memory address space extension device as claimed in claim 36, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

71. A memory address space extension device as claimed in claim 37, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

72. A memory address space extension device as claimed in claim 38, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

73. A memory address space extension device as claimed in claim 39, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

74. A memory address space extension device as claimed in claim 40, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

75. A memory address space extension device as claimed in claim 41, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

76. A memory address space extension device as claimed in claim 42, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

77. A memory address space extension device as claimed in claim 43, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

78. A memory address space extension device as claimed in claim 44, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to said interruption instruction according to software.

79. A memory address space extension device as claimed in claim 7, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

80. A memory address space extension device as claimed in claim 8, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

81. A memory address space extension device as claimed in claim 9, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

82. A memory address space extension device as claimed in claim 10, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

83. A memory address space extension device as claimed in claim 11, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

84. A memory address space extension device as claimed in claim 12, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

85. A memory address space extension device as claimed in claim 13, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

86. A memory address space extension device as claimed in claim 14, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

87. A memory address space extension device as claimed in claim 15, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

88. A memory address space extension device as claimed in claim 16, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

89. A memory address space extension device as claimed in claim 17, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

90. A memory address space extension device as claimed in claim 18, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

91. A memory address space extension device as claimed in claim 19, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

92. A memory address space extension device as claimed in claim 20, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

93. A memory address space extension device as claimed in claim 21, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

94. A memory address space extension device as claimed in claim 22, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

95. A memory address space extension device as claimed in claim 23, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

96. A memory address space extension device as claimed in claim 24, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

97. A memory address space extension device as claimed in claim 25, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

98. A memory address space extension device as claimed in claim 26, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

99. A memory address space extension device as claimed in claim 27, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

100. A memory address space extension device as claimed in claim 28, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

101. A memory address space extension device as claimed in claim 29, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

102. A memory address space extension device as claimed in claim 30, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

103. A memory address space extension device as claimed in claim 31, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

104. A memory address space extension device as claimed in claim 32, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

105. A memory address space extension device as claimed in claim 33, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

106. A memory address space extension device as claimed in claim 34, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

107. A memory address space extension device as claimed in claim 35, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

108. A memory address space extension device as claimed in claim 36, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

109. A memory address space extension device as claimed in claim 37, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

110. A memory address space extension device as claimed in claim 38, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

111. A memory address space extension device as claimed in claim 39, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

112. A memory address space extension device as claimed in claim 41, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

113. A memory address space extension device as claimed in claim 42, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

114. A memory address space extension device as claimed in claim 43, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

115. A memory address space extension device as claimed in claim 44, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

116. A memory address space extension device as claimed in claim 45, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

117. A memory address space extension device as claimed in claim 46, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

118. A memory address space extension device as claimed in claim 47, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

119. A memory address space extension device as claimed in claim 48, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

120. A memory address space extension device as claimed in claim 49, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

121. A memory address space extension device as claimed in claim 50, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

122. A memory address space extension device as claimed in claim 51, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

123. A memory address space extension device as claimed in claim 52, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

124. A memory address space extension device as claimed in claim 53, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

125. A memory address space extension device as claimed in claim 54, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

126. A memory address space extension device as claimed in claim 55, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

127. A memory address space extension device as claimed in claim 56, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

128. A memory address space extension device as claimed in claim 58, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

129. A memory address space extension device as claimed in claim 59, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

130. A memory address space extension device as claimed in claim 60, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

131. A memory address space extension device as claimed in claim 61, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

132. A memory address space extension device as claimed in claim 62, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

133. A memory address space extension device as claimed in claim 63, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

134. A memory address space extension device as claimed in claim 64, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

135. A memory address space extension device as claimed in claim 65, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

136. A memory address space extension device as claimed in claim 66, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

137. A memory address space extension device as claimed in claim 67, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

138. A memory address space extension device as claimed in claim 68, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

139. A memory address space extension device as claimed in claim 69, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

140. A memory address space extension device as claimed in claim 70, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory

having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

141. A memory address space extension device as claimed in claim 71, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

142. A memory address space extension device as claimed in claim 72, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

143. A memory address space extension device as claimed in claim 73, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area

according to said access right judgement means, before said memory with extended address supports said address operational means.

144. A memory address space extension device as claimed in claim 74, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

145. A memory address space extension device as claimed in claim 75, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

146. A memory address space extension device as claimed in claim 76, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

147. A memory address space extension device as claimed in claim 77, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

148. A memory address space extension device as claimed in claim 78, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

149. A memory address space extension device as claimed in claim 79, wherein there is further provided an address operational means for converting the CPU address into the extended address, and a memory having the extended address converted previously wherein said address operational means causes said CPU address to be converted into the extended address when said task is permitted to access to said data area according to said access right judgement means, before said memory with extended address supports said address operational means.

150. A storage medium storing therein a program in order to execute the processing of:

a definition table preparation processing for preparing said

definition table;

a reference processing for definition table which defines an access right of a task with respect to data area; and

an access right judgement processing for judging whether or not it causes the access right for the data area requested by a task to be given to said task according to said definition table.

151. A storage medium storing therein a program as claimed in claim 150, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every task ID given to said task.

152. A storage medium storing therein a program as claimed in claim 150, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every task ID given to said task and / or in every interruption number given to the interruption processing.

153. A storage medium storing therein a program as claimed in claim 150, wherein said access right judgement processing judges whether or not said task possesses the access right for accessing prescribed data area according to said task ID and / or said data area ID indicating the data area requested by said task.

154. A storage medium storing therein a program as claimed in claim 151, wherein said access right judgement processing judges whether or not said task possesses the access right for accessing prescribed data area according to said task ID and / or said data area ID

indicating the data area requested by said task.

155. A storage medium storing therein a program as claimed in claim 150, wherein said access right judgement processing judges whether or not said task possesses the access right for accessing prescribed data area according to any one of said task ID and said interruption processing number and / or said data area ID indicating the data area requested by said task.

156. A storage medium storing therein a program as claimed in claim 153, wherein said access right judgement processing judges whether or not said task possesses the access right for accessing prescribed data area according to any one of said task ID and said interruption processing number and / or said data area ID indicating the data area requested by said task.

157. A storage medium storing therein a program as claimed in claim 150, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

158. A storage medium storing therein a program as claimed in claim 151, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

159. A storage medium storing therein a program as claimed in claim 152, wherein said reference processing for definition table is the

reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

160. A storage medium storing therein a program as claimed in claim 153, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

161. A storage medium storing therein a program as claimed in claim 154, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

162. A storage medium storing therein a program as claimed in claim 155, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

163. A storage medium storing therein a program as claimed in claim 156, wherein said reference processing for definition table is the reference processing that it causes the definition table defining whether or not said task possesses the access right for accessing prescribed data area to be seen in every said task.

164. A storage medium storing therein a program as claimed in claim 150, wherein said reference processing for definition table is the

reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

165. A storage medium storing therein a program as claimed in claim 151, wherein said reference processing for definition table is the reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

166. A storage medium storing therein a program as claimed in claim 152, wherein said reference processing for definition table is the reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

167. A storage medium storing therein a program as claimed in claim 153, wherein said reference processing for definition table is the

reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

168. A storage medium storing therein a program as claimed in claim 154, wherein said reference processing for definition table is the reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

169. A storage medium storing therein a program as claimed in claim 155, wherein said reference processing for definition table is the reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

170. A storage medium storing therein a program as claimed in claim 156, wherein said reference processing for definition table is the

reference processing that it causes any one of:

(1) allowing only write of the data to be permitted;

(2) allowing read of the data to be permitted;

(3) allowing write of the data and read of the data to be permitted; and

(4) allowing no-access to be permitted,

to be seen with respect to said prescribed data area in every said task.

171. A storage medium storing therein a program as claimed in claim 152, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

172. A storage medium storing therein a program as claimed in claim 155, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

173. A storage medium storing therein a program as claimed in claim 156, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

174. A storage medium storing therein a program as claimed in claim 157, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

175. A storage medium storing therein a program as claimed in claim 158, wherein said program further executes interruption number

generation processing for generating interruption number to interruption processing according to hardware.

176. A storage medium storing therein a program as claimed in claim 159, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

177. A storage medium storing therein a program as claimed in claim 160, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

178. A storage medium storing therein a program as claimed in claim 161, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

179. A storage medium storing therein a program as claimed in claim 162, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

180. A storage medium storing therein a program as claimed in claim 163, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

181. A storage medium storing therein a program as claimed in claim 164, wherein said program further executes interruption number

generation processing for generating interruption number to interruption processing according to hardware.

182. A storage medium storing therein a program as claimed in claim 165, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

183. A storage medium storing therein a program as claimed in claim 166, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

184. A storage medium storing therein a program as claimed in claim 167, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

185. A storage medium storing therein a program as claimed in claim 168, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

186. A storage medium storing therein a program as claimed in claim 169, wherein said program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

187. A storage medium storing therein a program as claimed in claim 170, wherein said program further executes interruption number

generation processing for generating interruption number to interruption processing according to hardware.

188. A storage medium storing therein a program as claimed in claim 152, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

189. A storage medium storing therein a program as claimed in claim 155, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

190. A storage medium storing therein a program as claimed in claim 156, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

191. A storage medium storing therein a program as claimed in claim 157, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

192. A storage medium storing therein a program as claimed in claim 158, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption

instruction with respect to said interruption instruction according to software.

193. A storage medium storing therein a program as claimed in claim 159, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

194. A storage medium storing therein a program as claimed in claim 160, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

195. A storage medium storing therein a program as claimed in claim 161, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

196. A storage medium storing therein a program as claimed in claim 162, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

197. A storage medium storing therein a program as claimed in claim 163, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption

instruction with respect to said interruption instruction according to software.

198. A storage medium storing therein a program as claimed in claim 164, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

199. A storage medium storing therein a program as claimed in claim 165, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

200. A storage medium storing therein a program as claimed in claim 166, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

201. A storage medium storing therein a program as claimed in claim 167, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

202. A storage medium storing therein a program as claimed in claim 168, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption

instruction with respect to said interruption instruction according to software.

203. A storage medium storing therein a program as claimed in claim 169, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

204. A storage medium storing therein a program as claimed in claim 170, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

205. A storage medium storing therein a program as claimed in claim 171, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

206. A storage medium storing therein a program as claimed in claim 172, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

207. A storage medium storing therein a program as claimed in claim 173, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption

instruction with respect to said interruption instruction according to software.

208. A storage medium storing therein a program as claimed in claim 174, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

209. A storage medium storing therein a program as claimed in claim 175, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

210. A storage medium storing therein a program as claimed in claim 176, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

211. A storage medium storing therein a program as claimed in claim 177, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

212. A storage medium storing therein a program as claimed in claim 178, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption

instruction with respect to said interruption instruction according to software.

213. A storage medium storing therein a program as claimed in claim 179, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

214. A storage medium storing therein a program as claimed in claim 180, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

215. A storage medium storing therein a program as claimed in claim 181, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

216. A storage medium storing therein a program as claimed in claim 182, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

217. A storage medium storing therein a program as claimed in claim 183, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption

instruction with respect to said interruption instruction according to software.

218. A storage medium storing therein a program as claimed in claim 184, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

219. A storage medium storing therein a program as claimed in claim 185, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

220. A storage medium storing therein a program as claimed in claim 186, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

221. A storage medium storing therein a program as claimed in claim 187, wherein said program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

222. A storage medium storing therein a program as claimed in claim 150, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

223. A storage medium storing therein a program as claimed in claim 151, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

224. A storage medium storing therein a program as claimed in claim 152, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

225. A storage medium storing therein a program as claimed in claim 153, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address.

226. A storage medium storing therein a program as claimed in claim 154, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

227. A storage medium storing therein a program as claimed in claim 155, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

228. A storage medium storing therein a program as claimed in claim 156, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

229. A storage medium storing therein a program as claimed in claim 157, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

230. A storage medium storing therein a program as claimed in claim 158, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

231. A storage medium storing therein a program as claimed in claim 159, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

232. A storage medium storing therein a program as claimed in claim 160, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

233. A storage medium storing therein a program as claimed in claim 161, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

234. A storage medium storing therein a program as claimed in claim 162, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

235. A storage medium storing therein a program as claimed in claim 163, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address

236. A storage medium storing therein a program as claimed in claim 164, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

237. A storage medium storing therein a program as claimed in claim 165, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

238. A storage medium storing therein a program as claimed in claim 166, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

239. A storage medium storing therein a program as claimed in claim 167, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

240. A storage medium storing therein a program as claimed in claim 168, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

241. A storage medium storing therein a program as claimed in claim 169, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

242. A storage medium storing therein a program as claimed in claim 170, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

243. A storage medium storing therein a program as claimed in claim 171, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

244. A storage medium storing therein a program as claimed in claim 172, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

245. A storage medium storing therein a program as claimed in claim 173, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address.

246. A storage medium storing therein a program as claimed in claim 174, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

247. A storage medium storing therein a program as claimed in claim 175, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

248. A storage medium storing therein a program as claimed in claim 176, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

249. A storage medium storing therein a program as claimed in claim 177, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

250. A storage medium storing therein a program as claimed in claim 178, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

251. A storage medium storing therein a program as claimed in claim 179, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

252. A storage medium storing therein a program as claimed in claim 180, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

253. A storage medium storing therein a program as claimed in claim 181, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

254. A storage medium storing therein a program as claimed in claim 182, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

255. A storage medium storing therein a program as claimed in claim 183, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address.

256. A storage medium storing therein a program as claimed in claim 184, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

257. A storage medium storing therein a program as claimed in claim 185, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

258. A storage medium storing therein a program as claimed in claim 186, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

259. A storage medium storing therein a program as claimed in claim 187, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

260. A storage medium storing therein a program as claimed in claim 188, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

261. A storage medium storing therein a program as claimed in claim 189, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

262. A storage medium storing therein a program as claimed in claim 190, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

263. A storage medium storing therein a program as claimed in claim 191, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

264. A storage medium storing therein a program as claimed in claim 192, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

265. A storage medium storing therein a program as claimed in claim 193, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address.

266. A storage medium storing therein a program as claimed in claim 194, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

267. A storage medium storing therein a program as claimed in claim 195, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

268. A storage medium storing therein a program as claimed in claim 196, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

269. A storage medium storing therein a program as claimed in claim 197, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

270. A storage medium storing therein a program as claimed in claim 198, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

271. A storage medium storing therein a program as claimed in claim 199, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

272. A storage medium storing therein a program as claimed in claim 200, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

273. A storage medium storing therein a program as claimed in claim 201, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

274. A storage medium storing therein a program as claimed in claim 202, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

275. A storage medium storing therein a program as claimed in claim 203, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address.

276. A storage medium storing therein a program as claimed in claim 204, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

277. A storage medium storing therein a program as claimed in claim 205, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

278. A storage medium storing therein a program as claimed in claim 206, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

279. A storage medium storing therein a program as claimed in claim 207, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

280. A storage medium storing therein a program as claimed in claim 208, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

281. A storage medium storing therein a program as claimed in claim 209, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

282. A storage medium storing therein a program as claimed in claim 210, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

283. A storage medium storing therein a program as claimed in claim 211, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

284. A storage medium storing therein a program as claimed in claim 212, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

285. A storage medium storing therein a program as claimed in claim 213, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to

said access right judgement processing, before executing supporting processing by said memory with the extended address.

286. A storage medium storing therein a program as claimed in claim 214, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

287. A storage medium storing therein a program as claimed in claim 215, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

288. A storage medium storing therein a program as claimed in claim 216, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

289. A storage medium storing therein a program as claimed in claim 217, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

290. A storage medium storing therein a program as claimed in claim 218, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

291. A storage medium storing therein a program as claimed in claim 219, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

292. A storage medium storing therein a program as claimed in claim 220, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in

such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

293. A storage medium storing therein a program as claimed in claim 221, wherein said program executes an address operational processing in order to convert a CPU address into an extended address in such a way that said address operational processing causes said CPU address to be converted into said extended address when said task is judged that said task is permitted to access to said data area according to said access right judgement processing, before executing supporting processing by said memory with the extended address.

ABSTRACT OF THE DISCLOSURE

A memory address space extension device enables rewrite of data area caused by wrong access from the task to be prevented. A data area access right definition table is provided in a cache. The data area access right definition table defines whether or not a task (or interruption processing) during execution is permitted to access to a data area. An address operational unit extracts data area ID from a CPU address inputted from a CPU 1. A register bank control unit refers to above described definition table within the cache. The register bank control unit judges the access right of the task for the data area from both of a task ID (or interruption number of an interruption processing) of the task during execution stored in the ID register, and the data area ID extracted previously. When the access right is not permitted, system error occurs, while when the access right is permitted, processing for converting above-described CPU address into an extended address is implemented.

FIG. 1

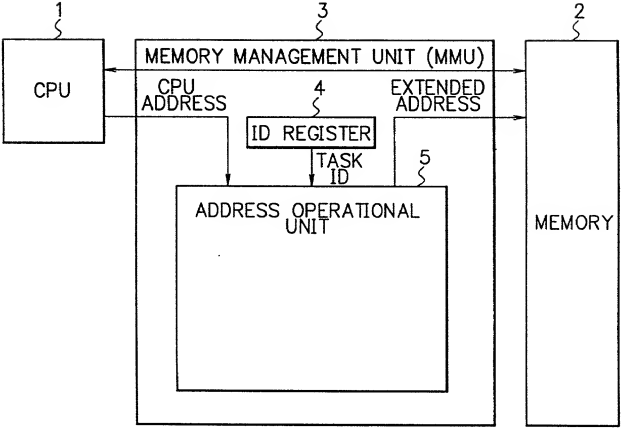

1
3
2
CPU
MEMORY MANAGEMENT UNIT (MMU)
CPU ADDRESS
4
EXTENDED ADDRESS
ID REGISTER
TASK ID
5
ADDRESS OPERATIONAL UNIT
MEMORY

FIG. 2

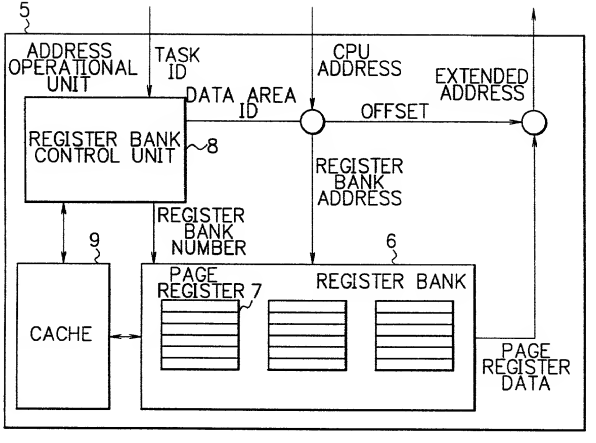


FIG. 3

REGISTER BANK SELECTION TABLE 10

DATA AREA ID	BANK NUMBER

FIG. 4

DATA AREA ACCESS RIGHT DEFINITION TABLE 11

TASK ID	AREA A	AREA B	AREA C		
1	O	×	O		
2	O	O	O		
3	×	O	×		
4	×	×	O		

× -------IN-PERMISSIBLE

O -------PERMISSIBLE

FIG. 5

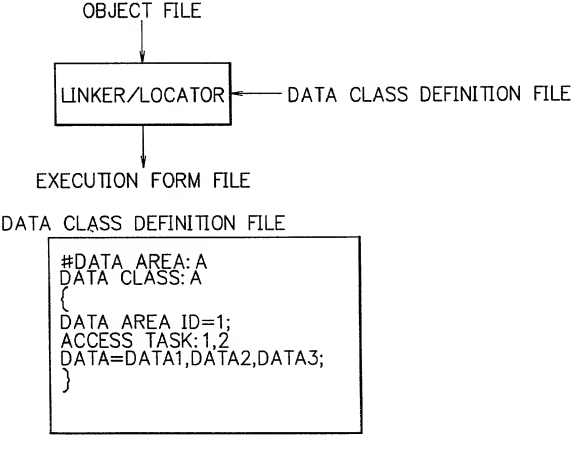


FIG. 6

DATA AREA ACCESS RIGHT DEFINITION TABLE 11

TASK ID	AREA A	AREA B	AREA C		
1	RW	X	RW		
2	R	R	R		
3	X	W	X		
4	X	X	R		

R---- READABLE, IN-WRITABLE,
W---- IN-READABLE, WRITABLE,
RW---- READABLE, WRITABLE,
X---- IN-READABLE, IN-WRITABLE

F I G. 7

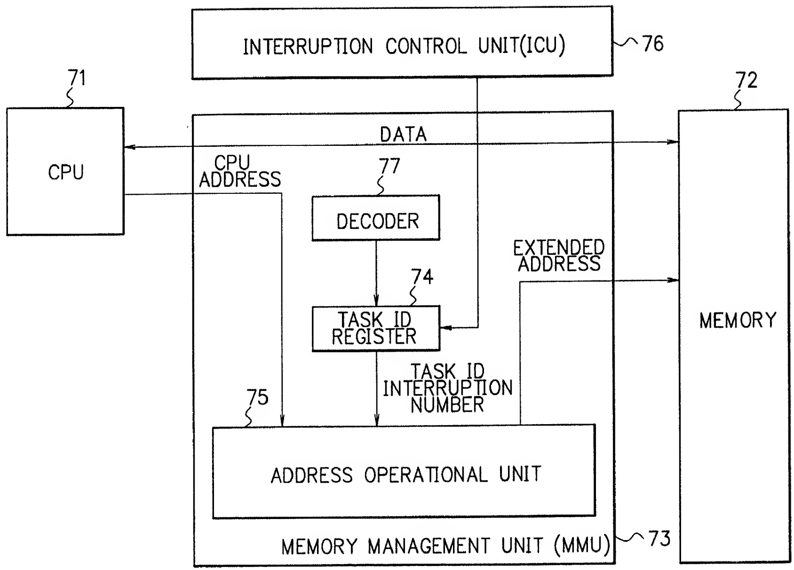

INTERRUPTION CONTROL UNIT(ICU)
76
71
72
CPU
DATA
CPU ADDRESS
77
DECODER
74
TASK ID REGISTER
EXTENDED ADDRESS
MEMORY
TASK ID INTERRUPTION NUMBER
75
ADDRESS OPERATIONAL UNIT
MEMORY MANAGEMENT UNIT (MMU)
73

FIG. 8

DATA AREA ACCESS RIGHT DEFINITION TABLE 81

TASK ID OR INTERRUPTION NUMBER	AREA A	AREA B	AREA C		
1	O	×	O		
2	O	X	X		
3	X	O	X		
101	O	X	O		
102	O	O	O		
103	X	O	X		
104	X	X	O		

FIG. 9

DATA AREA ACCESS RIGHT DEFINITION TABLE 91

TASK ID OR INTERRUPTION NUMBER	AREA A	AREA B	AREA C		
1	R	X	R		
2	RW	X	X		
3	X	W	X		
101	RW	X	RW		
102	R	R	R		
103	X	W	X		
104	X	X	R		

FIG. 10

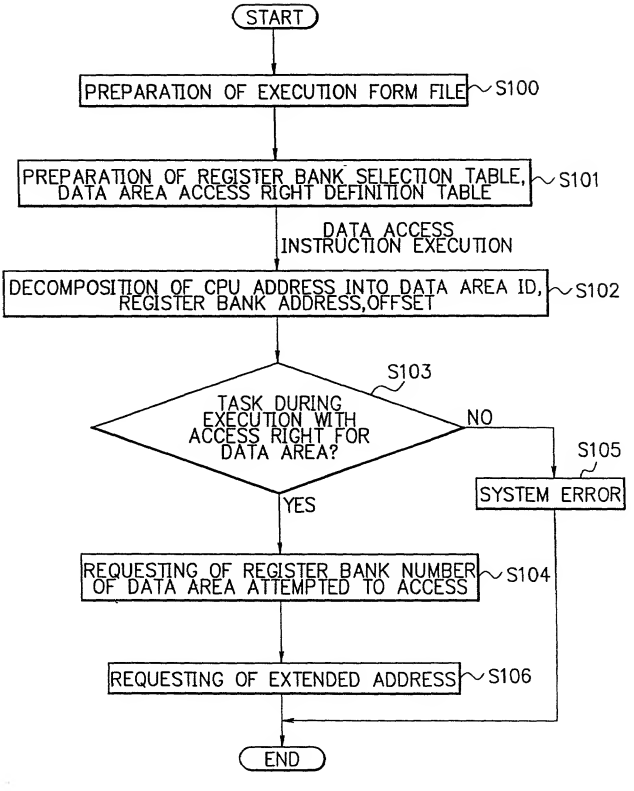
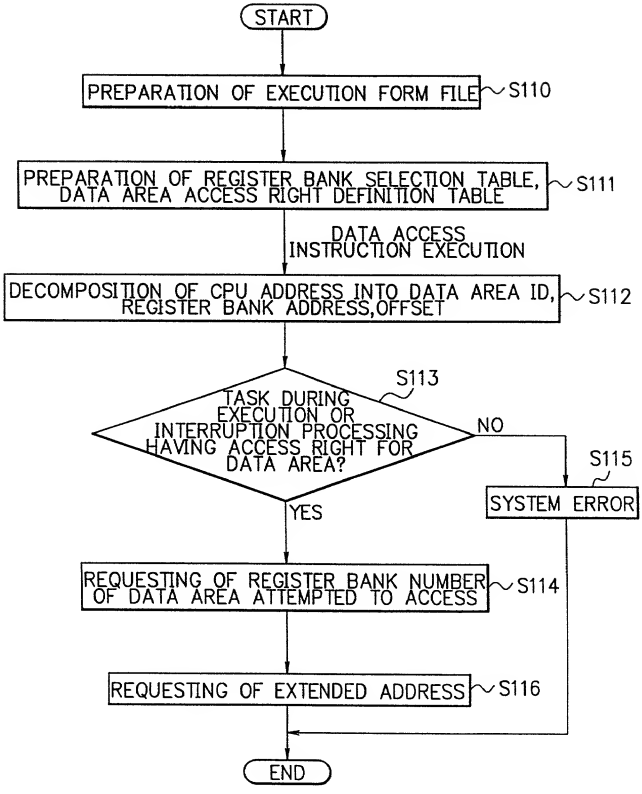

START
PREPARATION OF EXECUTION FORM FILE
S100
PREPARATION OF REGISTER BANK SELECTION TABLE, DATA AREA ACCESS RIGHT DEFINITION TABLE
S101
DATA ACCESS INSTRUCTION EXECUTION
DECOMPOSITION OF CPU ADDRESS INTO DATA AREA ID, REGISTER BANK ADDRESS, OFFSET
S102
S103
TASK DURING EXECUTION WITH ACCESS RIGHT FOR DATA AREA?
NO
S105
SYSTEM ERROR
YES
REQUESTING OF REGISTER BANK NUMBER OF DATA AREA ATTEMPTED TO ACCESS
S104
REQUESTING OF EXTENDED ADDRESS
S106
END

FIG. 11


START
PREPARATION OF EXECUTION FORM FILE
S110
PREPARATION OF REGISTER BANK SELECTION TABLE, DATA AREA ACCESS RIGHT DEFINITION TABLE
S111
DATA ACCESS INSTRUCTION EXECUTION
DECOMPOSITION OF CPU ADDRESS INTO DATA AREA ID, REGISTER BANK ADDRESS,OFFSET
S112
S113
TASK DURING EXECUTION OR INTERRUPTION PROCESSING HAVING ACCESS RIGHT FOR DATA AREA?
NO
S115
SYSTEM ERROR
YES
REQUESTING OF REGISTER BANK NUMBER OF DATA AREA ATTEMPTED TO ACCESS
S114
REQUESTING OF EXTENDED ADDRESS
S116
END

UNITED STATES OF AMERICA
COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

OFGS FILE NO. P/1909-130

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY ADDRESS SPACE EXTENSION DEVICE AND STORAGE MEDIUM STORING THEREIN PROGRAM THEREOF

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	112368/1999	20, 4, 1999	YES X NO ____
Japan	014102/2000	19, 1, 2000	YES X NO ____
			YES ____ NO ____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby appoint OSTROLENK, FABER, GERB & SOFFEN, and the members of the firm, Marvin C. Soffen - Reg. No. 17,542; Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944 and Louis C. Dujmich - Reg. No. 30,625, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

SEND CORRESPONDENCE TO: OSTROLENK, FABER, GERB & SOFFEN
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(212) 382-0700

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE	DATE
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FULL NAME OF SECOND JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE
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POST OFFICE ADDRESS		
FULL NAME OF THIRD JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE
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